

Picoampere Input Current Bipolar Op Amp

AD705

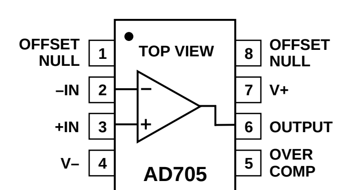
FEATURES
DC PERFORMANCE
25 μV max Offset Voltage (AD705T)
0.6 μV/°C max Drift (AD705K/T)
100 pA max Input Bias Current (AD705K)
600 pA max I_B Over MIL Temperature Range (AD705T)
114 dB min CMRR (AD705K/T)
114 dB min PSRR (AD705T)
200 V/mV min Open Loop Gain
0.5 μV p-p typ Noise, 0.1 Hz to 10 Hz
600 μA max Supply Current

AC PERFORMANCE
0.15 V/μs Slew Rate
800 kHz Unity Gain Crossover Frequency
10,000 pF Capacitive Load Drive Capability
Low Cost
Available in 8-Pin Plastic Mini-DIP, Hermetic Cerdip and Surface Mount (SOIC) Packages
MIL-STD-883B Processing Available
Dual Version Available: AD706
Quad Version: AD704

APPLICATIONS
Low Frequency Active Filters
Precision Instrumentation
Precision Integrators

CONNECTION DIAGRAM

Plastic Mini-DIP (N)
Cerdip (Q) and
Plastic SOIC (R) Packages



PRODUCT DESCRIPTION

The AD705 is a low power bipolar op amp that has the low input bias current of a BiFET amplifier but which offers a significantly lower I_B drift over temperature. The AD705 offers many of the advantages of BiFET and bipolar op amps without their inherent disadvantages. It utilizes superbeta bipolar input transistors to achieve the picoampere input bias current levels of FET input amplifiers (at room temperature), while its I_B typically only increases 5 times vs. BiFET amplifiers which exhibit a 1000X increase over temperature. This means that, at room temperature, while a typical BiFET may have less I_B than the AD705, the BiFET's input current will increase to a level of several nA at +125°C. Superbeta bipolar technology also permits the AD705 to achieve the microvolt offset voltage and low noise characteristics of a precision bipolar input amplifier.

The AD705 is a high quality replacement for the industry-standard OP07 amplifier while drawing only one sixth of its power supply current. Since it has only 1/20th the input bias current of an OP07, the AD705 can be used with much higher source impedances, while providing the same level of dc precision. In addition, since the input bias currents are at picoAmp levels, the commonly used "balancing" resistor (connected between the noninverting input of a bipolar op amp and ground) is not required.

The AD705 is an excellent choice for use in low frequency active filters in 12- and 14-bit data acquisition systems, in precision instrumentation and as a high quality integrator.

The AD705 is internally compensated for unity gain and is available in five performance grades. The AD705J and AD705K are rated over the commercial temperature range of 0°C to +70°C. The AD705A and AD705B are rated over the industrial temperature range of –40°C to +85°C. The AD705T is rated over the military temperature range of –55°C to +125°C and is available processed to MIL-STD-883B, Rev. C.

The AD705 is offered in three varieties of 8-pin package: plastic DIP, hermetic cerdip and surface mount (SOIC). "J" grade chips are also available.

PRODUCT HIGHLIGHTS

1. The AD705 is a low drift op amp that offers BiFET level input bias currents, yet has the low I_B drift of a bipolar amplifier. It upgrades the performance of circuits using op amps such as the LT1012.
2. The combination of Analog Devices' advanced superbeta processing technology and factory trimming provides both low drift and high dc precision.
3. The AD705 can be used in applications where a chopper amplifier would normally be required but without the chopper's inherent noise and other problems.

REV. B

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Tel: 617/329-4700 **Fax: 617/326-8703**

AD705–SPECIFICATIONS (@ T_A = +25°C, V_{CM} = 0 V, and V_S = ±15 V dc, unless otherwise noted)

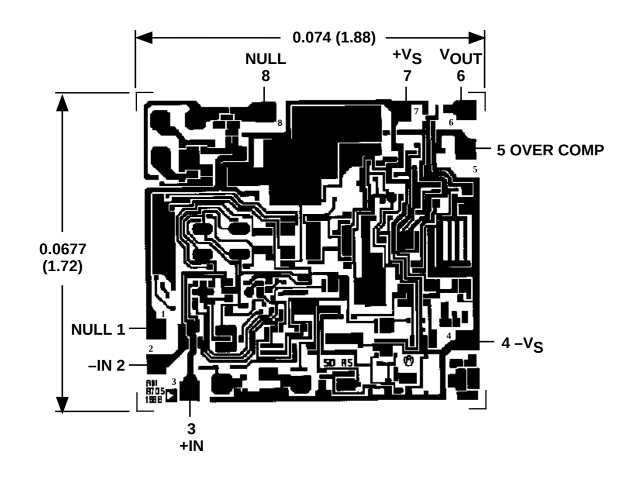
Parameter	Conditions	AD705J/A Min	AD705J/A Typ	AD705J/A Max	AD705K/B Min	AD705K/B Typ	AD705K/B Max	AD705T Min	AD705T Typ	AD705T Max	Units
INPUT OFFSET VOLTAGE											
Initial Offset			30	**90**		10	**35**		10	**25**	µV
Offset	T_{MIN} to T_{MAX}		45	150		25	**60**		25	**60**	µV
vs. Temp, Average TC			0.2	1.2		0.2	0.6		0.2	**0.6**	µV/°C
vs. Supply (PSRR)	V_S = ±2 V to ±18 V	**110**	129		**110**	129		**114**	129		dB
T_{MIN} to T_{MAX}	V_S = ±2.5 V to ±18 V	108	126		108	126		**108**	126		dB
Long Term Stability			0.3			0.3			0.3		µV/month
INPUT BIAS CURRENT[1]											
	V_{CM} = 0 V		60	**150**		30	**100**		30	**100**	pA
	V_{CM} = ±13.5 V		80	200		50	**150**		50	**150**	pA
vs. Temp, Average TC			0.3			0.3			0.6		pA/°C
T_{MIN} to T_{MAX}	V_{CM} = 0 V		80	250		50	150		90	**600**	pA
T_{MIN} to T_{MAX}	V_{CM} = ±13.5 V		100	450		70	350		120	**750**	pA
INPUT OFFSET CURRENT	V_{CM} = 0 V		40	**150**		30	**100**		30	**100**	pA
	V_{CM} = ±13.5 V		40	200		30	**150**		30	**150**	pA
vs. Temp, Average TC			0.3			0.3			0.4		pA/°C
T_{MIN} to T_{MAX}	V_{CM} = 0 V		80	250		50	150		80	**250**	pA
T_{MIN} to T_{MAX}	V_{CM} = ±13.5 V		80	450		50	350		80	**450**	pA
FREQUENCY RESPONSE											
Unity Gain Crossover Frequency		0.4	0.8		0.4	0.8		0.4	0.8		MHz
Slew Rate, Unity Gain	G = –1	0.1	0.15		0.1	0.15		0.1	0.15		V/µs
Slew Rate	T_{MIN} to T_{MAX}	0.05	0.15		0.05	0.15		0.05	0.15		V/µs
INPUT IMPEDANCE											
Differential			40‖2			40‖2			40‖2		MΩ‖pF
Common Mode			300‖2			300‖2			300‖2		GΩ‖pF
INPUT VOLTAGE RANGE											
Common-Mode Voltage		±13.5	±14		±13.5	±14		±13.5	±14		V
COMMON-MODE REJECTION RATIO	V_{CM} = ±13.5 V	**110**	132		**114**	132		**114**	132		dB
	T_{MIN} to T_{MAX}	108	128		108	128		**108**	128		dB
INPUT VOLTAGE NOISE	0.1 Hz to 10 Hz		0.5			0.5	1.0		0.5	1.0	µV p-p
	f = 10 Hz		17			17			17		nV/√Hz
	f = 1 kHz		15	22		15	22		15	22	nV/√Hz
INPUT CURRENT NOISE	f = 10 Hz		50			50			50		fA/√Hz
OPEN-LOOP GAIN	V_O = ±12 V										
	R_{LOAD} = 10 kΩ	**300**	2000		**400**	2000		**400**	2000		V/mV
	T_{MIN} to T_{MAX}	200	1500		300	1500		300	1500		V/mV
	V_O = ±10 V										
	R_{LOAD} = 2 kΩ	**200**	1000		**300**	1000		**300**	1000		V/mV
	T_{MIN} to T_{MAX}	150	1000		200	1000		**200**	1000		V/mV
OUTPUT CHARACTERISTICS											
Voltage Swing	R_{LOAD} = 10 kΩ	±13	±14		±13	±14		±13	±14		V
	T_{MIN} to T_{MAX}	**±13**	±14		**±13**	±14		**±13**	±14		V
Current	Short Circuit		±15			±15			±15		mA
Capacitive Load Drive Capability	Gain = +1		10,000			10,000			10,000		pF
Output Resistance	Open Loop		200			200			200		Ω
POWER SUPPLY											
Rated Performance			±15			±15			±15		V
Operating Range		**±2.0**		**±18**	**±2.0**		**±18**	**±2.0**		**±18**	V
Quiescent Current			380	**600**		380	**600**		380	**600**	µA
	T_{MIN} to T_{MAX}		400	800		400	800		400	**800**	µA
TEMPERATURE RANGE FOR RATED PERFORMANCE											
Commercial (0°C to +70°C)			AD705J			AD705K					
Industrial (–40°C to +85°C)			AD705A			AD705B					
Military (–55°C to +125°C)									AD705T		

Parameter	Conditions	AD705J/A Min	AD705J/A Typ	AD705J/A Max	AD705K/B Min	AD705K/B Typ	AD705K/B Max	AD705T Min	AD705T Typ	AD705T Max	Units
PACKAGE OPTIONS											
8-Pin Cerdip (Q-8)			AD705AQ			AD705BQ			AD705TQ		
8-Pin Plastic Mini-DIP (N-8)			AD705JN			AD705KN					
8-Pin SOIC (R-8)			AD705JR								
Chips			AD705JCHIPS								
TRANSISTOR COUNT	# of Transistors		45			45			45		

NOTES
[1]Bias current specifications are guaranteed maximum at either input.
All min and max specifications are guaranteed
Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.
Specifications subject to change without notice.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±18 V
Internal Power Dissipation[2] . . . . 650 mW
Input Voltage . . . . $\pm V_S$
Differential Input Voltage[3] . . . . ±0.7 V
Output Short Circuit Duration . . . . Indefinite
Storage Temperature Range (N, R) . . . . –65°C to +125°C
Storage Temperature Range (Q) . . . . –65°C to +150°C
Operating Temperature Range
AD705J/K . . . . 0°C to +70°C
AD705A/B . . . . –40°C to +85°C
AD705T . . . . –55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
8-Pin Plastic Package: θ_{JA} = 165°C/Watt
8-Pin Cerdip Package: θ_{JA} = 110°C/Watt
8-Pin Small Outline Package: θ_{JA} = 155°C/Watt
[3]The input pins of these amplifiers are protected by back-to-back diodes. If the differential voltage exceeds ±0.7 V, external series protection resistors should be added to limit the input current to less than 25 mA.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD705AQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD705BQ	–40°C to +85°C	8-Pin Ceramic DIP	Q-8
AD705JCHIPS	0°C to +70°C	Bare Die	
AD705JN	0°C to +70°C	8-Pin Plastic DIP	N-8
AD705JR	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD705JR-REEL	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD705JR-REEL7	0°C to +70°C	8-Pin Plastic SOIC	R-8
AD705KN	0°C to +70°C	8-Pin Plastic DIP	N-8
AD705TQ	–55°C to +125°C	8-Pin Ceramic DIP	Q-8
AD705TQ/883B	–55°C to +125°C	8-Pin Ceramic DIP	Q-8

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD705 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



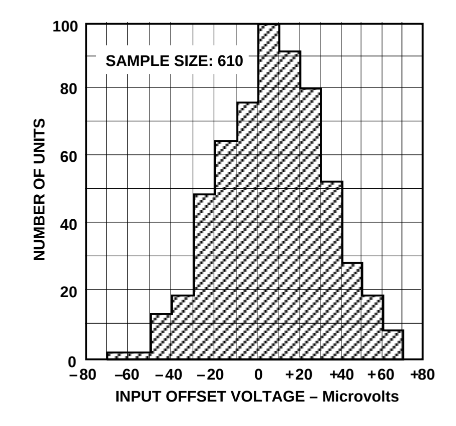


Figure 1. Typical Distribution of Input Offset Voltage

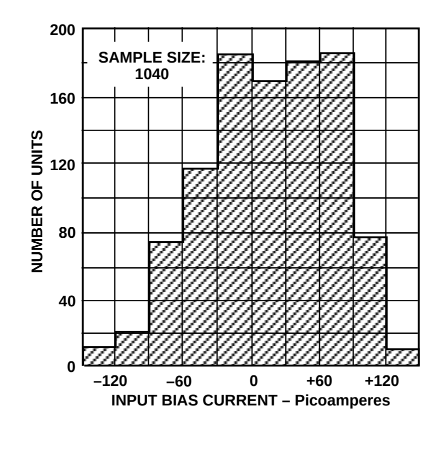


Figure 2. Typical Distribution of Input Bias Current

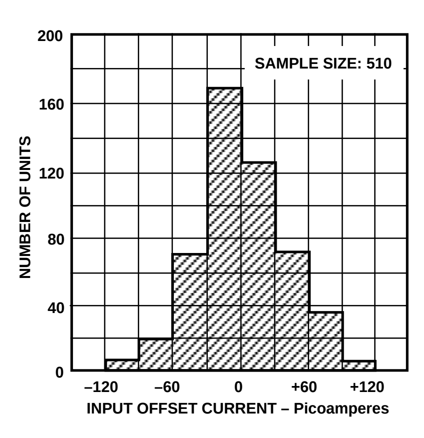


Figure 3. Typical Distribution of Input Offset Current

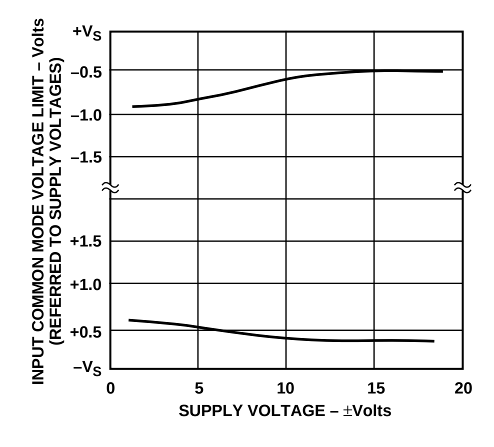


Figure 4. Input Common-Mode Voltage Range vs. Supply Voltage

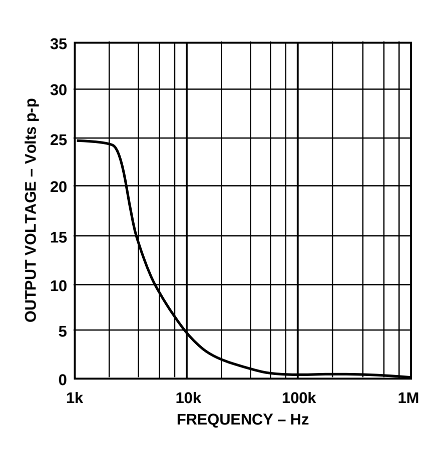


Figure 5. Large Signal Frequency Response

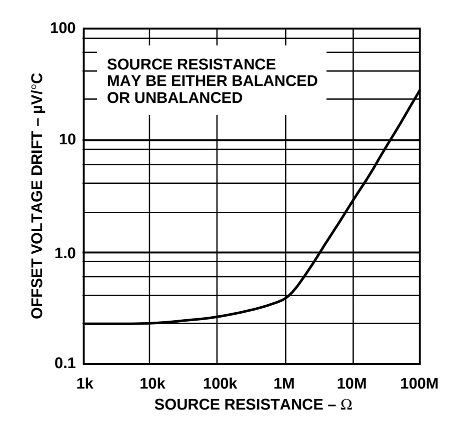


Figure 6. Offset Voltage Drift vs. Source Resistance

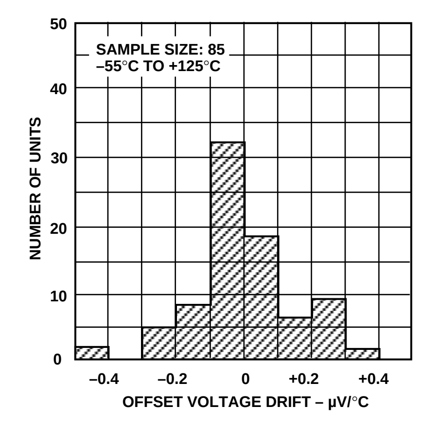


Figure 7. Typical Distribution of Offset Voltage Drift

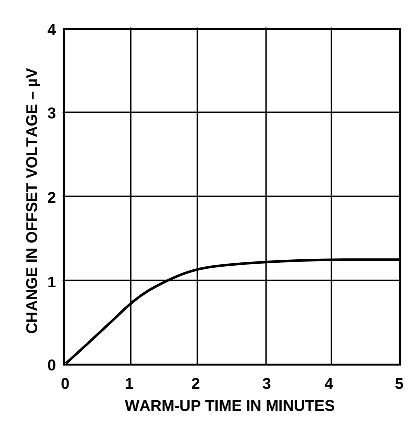


Figure 8. Change in Input Offset Voltage vs. Warm-Up Time

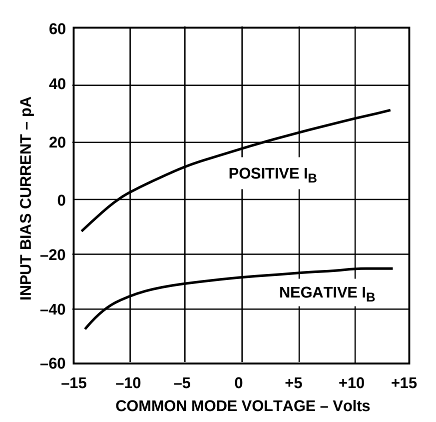


Figure 9. Input Bias Current vs. Common-Mode Voltage

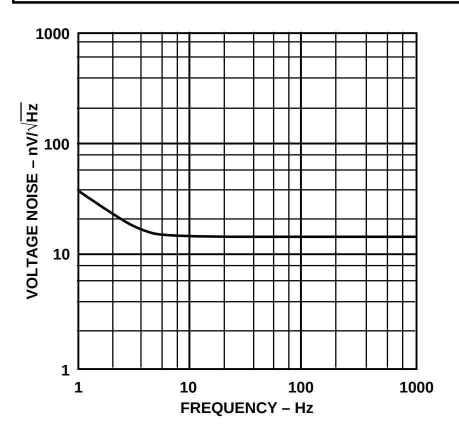


Figure 10. Input Noise Voltage Spectral Density

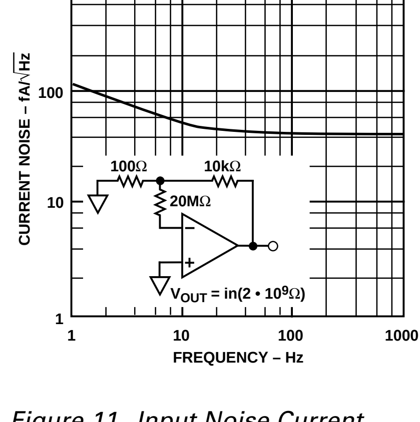


Figure 11. Input Noise Current Spectral Density

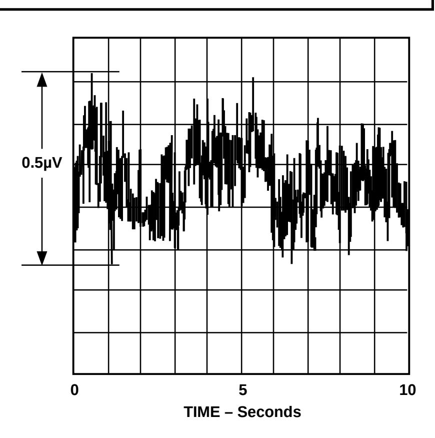


Figure 12. 0.1 Hz to 10 Hz Noise Voltage

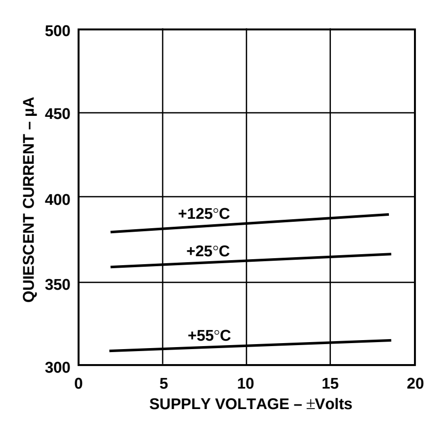


Figure 13. Quiescent Supply Current vs. Supply Voltage

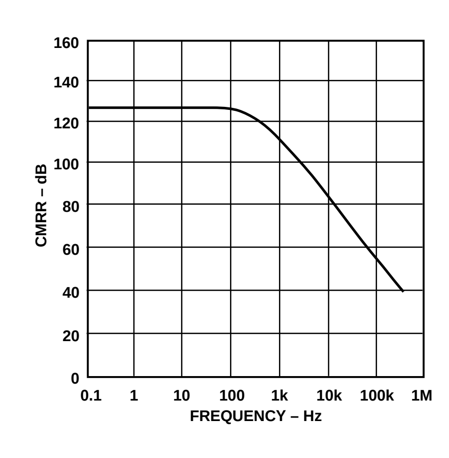


Figure 14. Common-Mode Rejection vs. Frequency

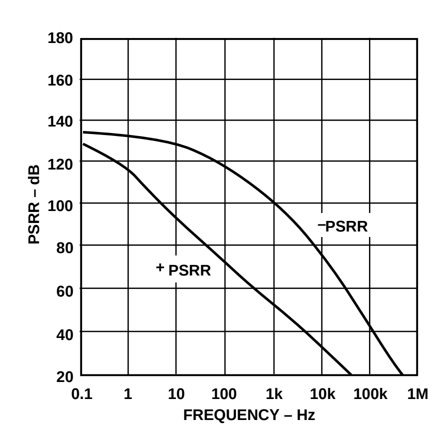


Figure 15. Power Supply Rejection vs. Frequency

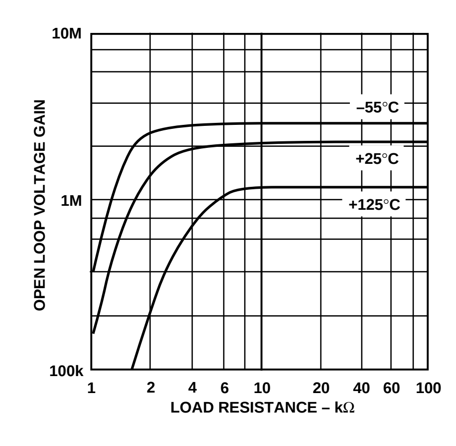


Figure 16. Open Loop Gain vs. Load Resistance over Temperature

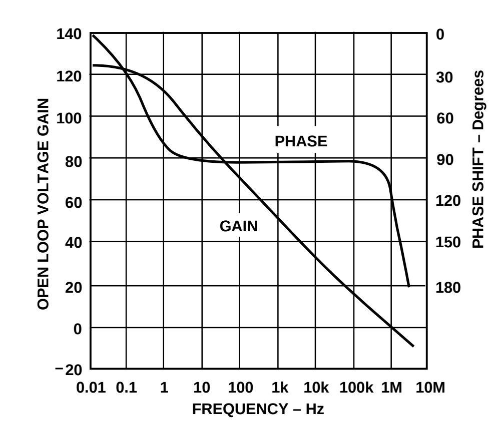


Figure 17. Open Loop Gain and Phase Shift vs. Frequency

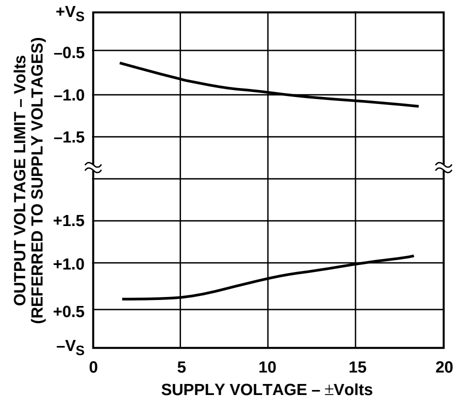


Figure 18. Output Voltage Limit vs. Supply Voltage

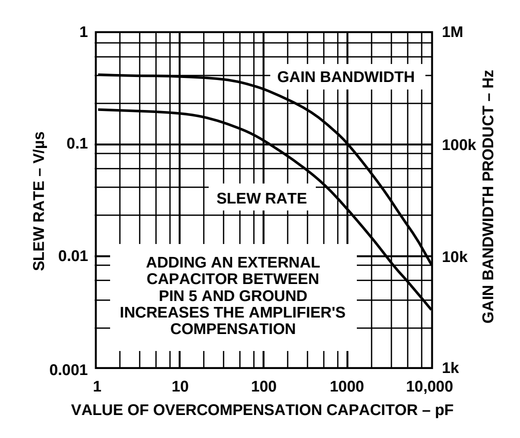


Figure 19. Slew Rate & Gain Bandwidth Product vs. Value of Overcompensation Capacitor

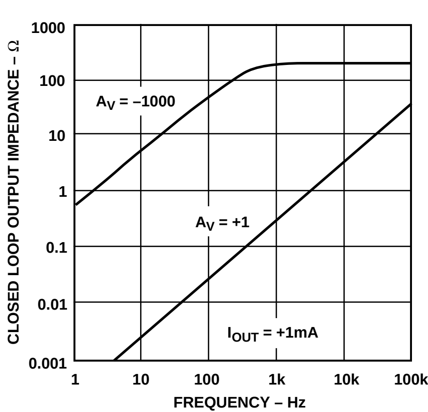


Figure 20. Magnitude of Closed Loop Output Impedance vs. Frequency

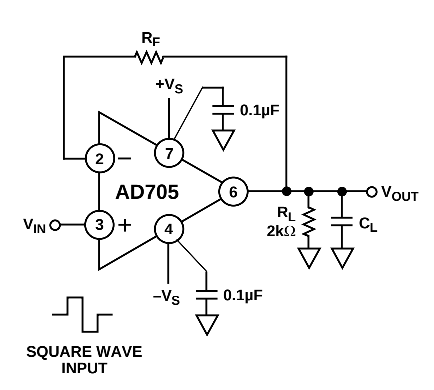


Figure 21a. Unity Gain Follower (For Large Signal Applications, Resistor R_F Limits the Current Through the Input Protection Diodes)

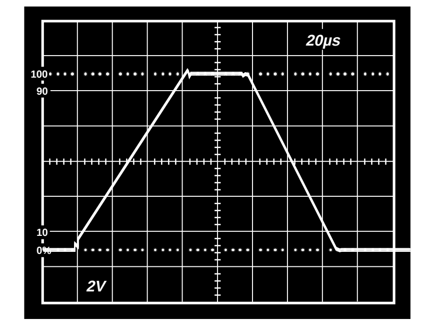


Figure 21b. Unity Gain Follower Large Signal Pulse Response R_F = 10 kΩ, C_L = 50 pF

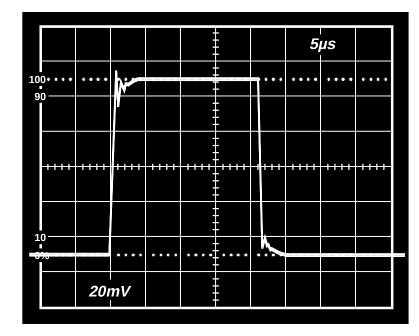


Figure 21c. Unity Gain Follower Small Signal Pulse Response R_F = 0 Ω, C_L = 100 pF

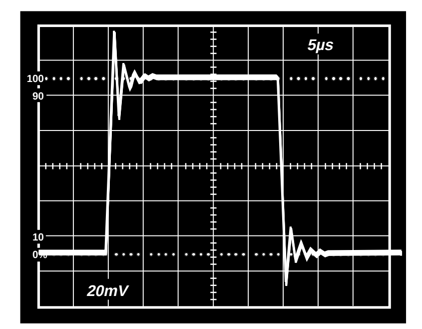


Figure 21d. Unity Gain Follower Small Signal Pulse Response R_F = 0 Ω, C_L = 1000 pF

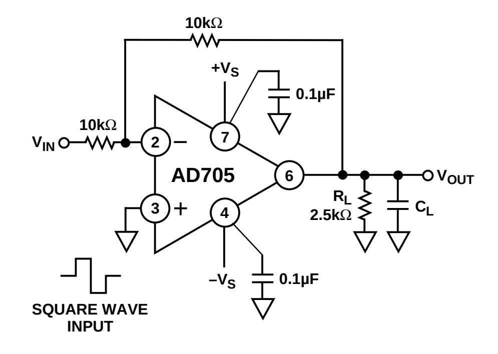


Figure 22a. Unity Gain Inverter

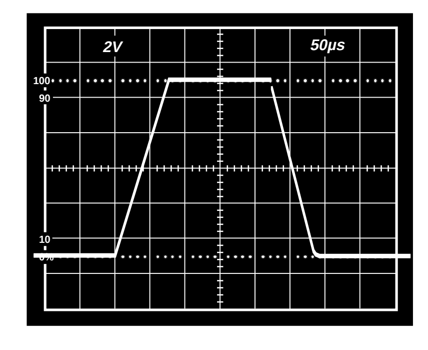


Figure 22b. Unity Gain Inverter Large Signal Pulse Response C_L = 50 pF

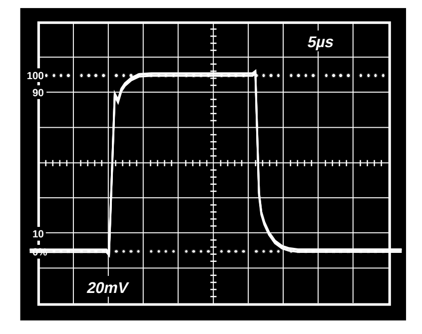


Figure 22c. Unity Gain Inverter Small Signal Pulse Response C_L = 100 pF

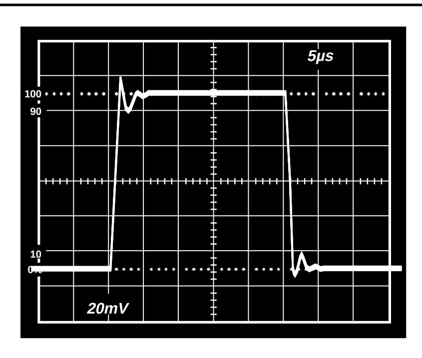


Figure 22d. Unity Gain Inverter Small Signal Pulse Response C, = 1000 pF

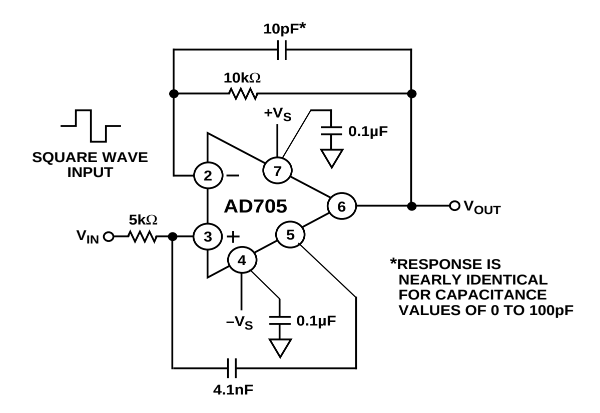


Figure 23a. Follower Connected in Feed-Forward Mode

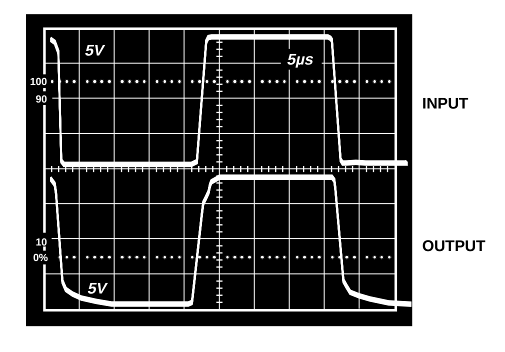


Figure 23b. Follower Feed-Forward Pulse Response

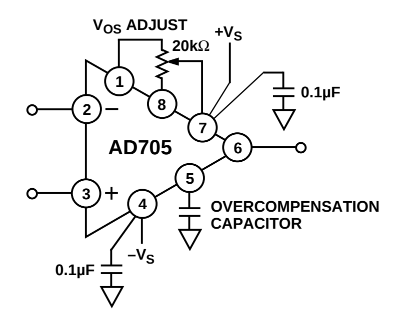


Figure 24. Offset Null and Overcompensation Connections

A High Performance Differential Amplifier Circuit

Figure 25 shows a high input impedance, differential amplifier circuit that features a high common-mode voltage, and which operates at low power. Table I details its performance with changes in gain. To optimize the common-mode rejection of this circuit at low frequencies and dc, apply a 1 volt, 1 Hz sine wave to both inputs. Measuring the output with an oscilloscope, adjust trimming potentiometer R6 for minimum output. For the best CMR at higher frequencies, capacitor C2 should be replaced with a 1.5 pF to 20 pF trimmer capacitor.

Both the IC socket and any standoffs at the op amp's input terminals should be made of Teflon* to maintain low input current drift over temperature.

*Teflon is a registered trademark of E.I. DuPont, Co.

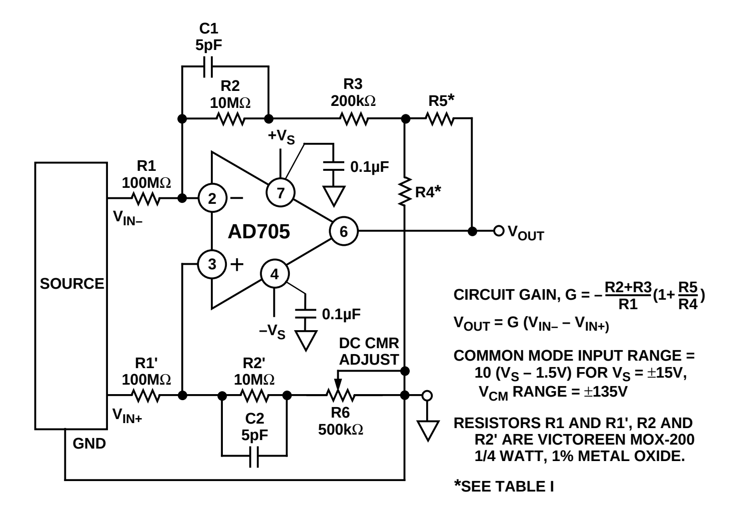


Figure 25. A High Performance Differentials Amplifier Circuit

Table I. Typical Performance of Differential Amplifier Circuit Operating at Various Gains

Circuit Gain	R4 (Ω)	R5 (Ω)	Trimmed DC CMR (dB)	RTI Average Drift TC (µV/°C)	Circuit Bandwidth –3 dB
1	1.13 kΩ	10 kΩ	≥85	30	4.4 kHz
10	100 Ω	9.76 kΩ	≥85	30	2.8 kHz
100	10.2 Ω	10 kΩ	≥85	30	930 Hz

A 1 Hz, 2-Pole, Active Filter

Table II gives recommended component values for the 1 Hz filter of Figure 26. An unusual characteristic of the AD705 is that both the input bias current and the input offset current and their drift remain low over most of the op amps rated temperature range. Therefore, for most applications, there is no need to use the normal balancing resistor tied between the noninverting terminal of the op amp and ground. Eliminating the standard balancing resistor reduces board space and lowers circuit noise. However, this resistor is needed at temperatures above 110°C, because input bias current starts to change rapidly, as shown by Figure 27.

Table II. Recommended Component Values for the 1 Hz Low-Pass Filter

Desired Low Pass Response	Pole Frequency (Hz)	Pole Q	C1 Value (μF)	C2 Value (μF)
Bessel Response	1.27	0.58	0.14	0.11
Butterworth Response	1.00	0.707	0.23	0.11
0.1 dB Chebychev	0.93	0.77	0.26	0.11
0.2 dB Chebychev	0.90	0.80	0.28	0.11
0.5 dB Chebychev	0.85	0.86	0.32	0.11
1.0 dB Chebychev	0.80	0.96	0.38	0.10

Specified values are for a –3 dB point of 1.0 Hz. For other frequencies, simply scale capacitors C1 and C2 directly; i.e., for 3 Hz Bessel response, C1 = 0.046 μF, C2 = 0.037 μF.

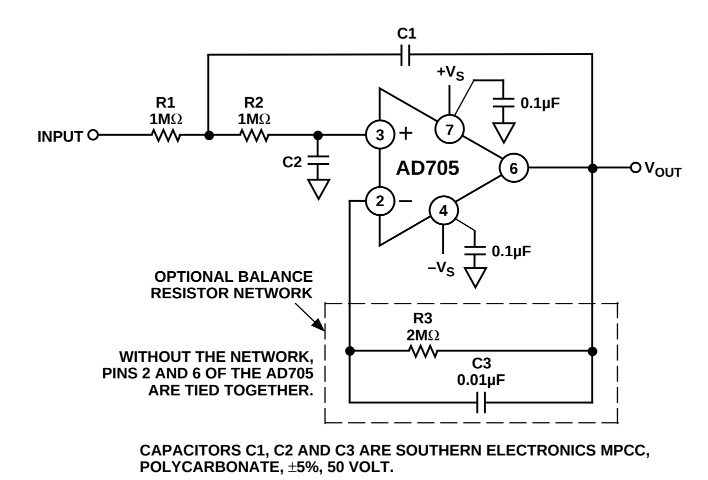


Figure 26. A 1 Hz, 2-Pole Active Filter

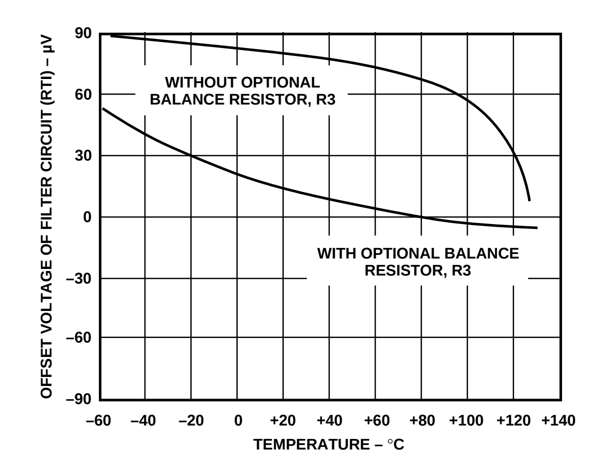
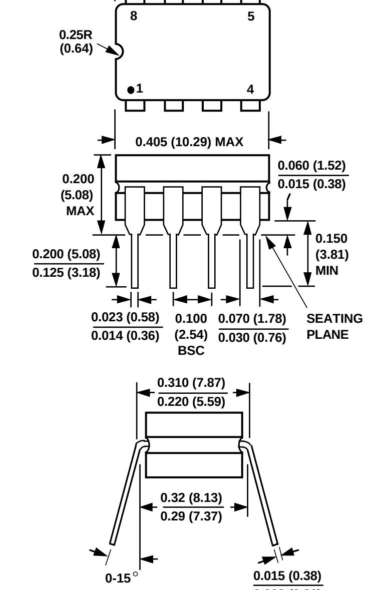


Figure 27. V_{OS} vs. Temperature of 1 Hz Filter

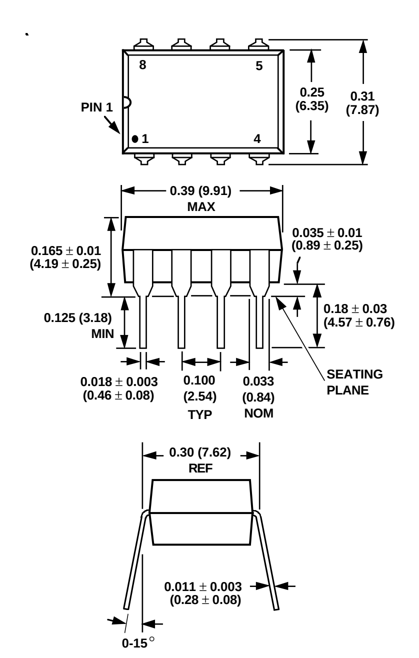
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

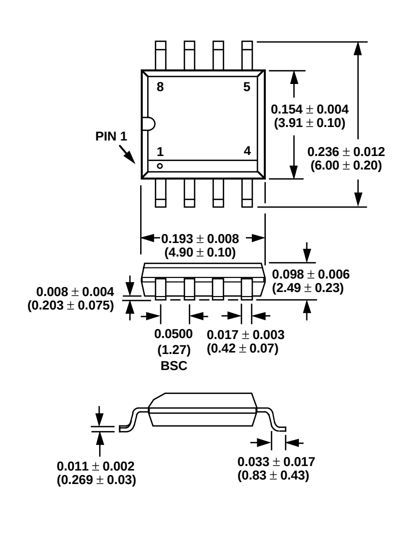
Cerdip (Q) Package



Plastic Mini-DIP (N) Package



8-Pin SOIC (R) Package



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